

What is claimed is:

1 1. A test device for detecting alignment of deep
2 trench capacitors and word lines in DRAM devices with
3 vertical transistors, wherein the test device is disposed
4 in a scribe line region of a wafer, comprising:

5 an active area disposed in the scribe line region;

6 an H-type deep trench capacitor disposed in the
7 active area, having parallel first and second
8 portions and a third portion, wherein each of
9 the first and second portions has a center and
10 two ends, and the third portion is disposed
11 between the centers of the first and second
12 portions;

13 first to fourth conductive pads disposed on the two
14 ends of the first and second portions
15 respectively; and

16 a bar-type conductive pad disposed between the first
17 and second portions, having a center aligned
18 with a center of the third portion.

1 2. The test device as claimed in claim 1, wherein
2 the first to fourth conductive pads and the bar-type
3 conductive pad are made of the same material.

1 3. The test device as claimed in claim 1, wherein
2 the first to fourth conductive pads and the bar-type
3 conductive pad are made of polysilicon.

1 4. The test device as claimed in claim 1, wherein
2 the bar-type conductive pad, the first portion and the
3 second portion are parallel.

1 5. A method for detecting alignment of deep trench
2 capacitors and word lines in DRAM devices with vertical
3 transistors, comprising:

4 providing a wafer with at least one scribe line
5 region and at least one memory region;

6 forming a plurality of memory cells with vertical
7 transistors in the memory region and at least
8 one test device in the scribe line
9 simultaneously, wherein the memory cells have
10 word line areas and deep trench capacitors, the
11 test device including:

12 an active area disposed in the scribe line
13 region;

14 an H-type deep trench capacitor disposed in the
15 active area, having parallel first and
16 second portions and a third portion,
17 wherein each of the first and second
18 portions has a center and two ends, and
19 the third portion is disposed between the
20 centers of the first and second portions;

21 first to fourth conductive pads disposed on the
22 two ends of the first and second portions
23 respectively; and

24 a bar-type conductive pad disposed between the
25 first and second portions, having a center

26 aligned with a center of the third
27 portion;
28 detecting a first resistance between the first
29 conductive pad disposed on the first portion
30 and the bar-type conductive pad, and a second
31 resistance between the second conductive pad
32 disposed on the second portion and the bar-type
33 conductive pad;
34 determining alignment of the H-type deep trench
35 capacitor and the bar-type conductive pad
36 according to the first resistance and the
37 second resistance; and
38 determining alignment of the deep trench capacitors
39 and word lines in the memory regions according
40 to alignment of the H-type deep trench
41 capacitor and the bar-type conductive pad of
42 the test device.

1 6. The method as claimed in claim 5, wherein the
2 bar-type conductive pad is a predetermined distance from
3 the first and second portions.

1 7. The method as claimed in Claim 6, further
2 comprising a step of determining alignment shift (ΔL) of
3 the H-type deep trench capacitor and the bar-type
4 conductive pad area according to the first resistance,
5 the second resistance, and the predetermined distance
6 between first and second portions and the bar-type
7 conductive pad respectively.

1 8. The method as claimed in Claim 7, wherein the
2 alignment shift (ΔL) is determined by an equation:

3
$$\Delta L = L \times \frac{(R2 - R1)}{(R2 + R1)};$$

4 wherein L is the predetermined distance between
5 first and second portions and the bar-type
6 conductive pad respectively; R1 is the first
7 resistance between the first conductive pad
8 disposed on the first portion and the bar-type
9 conductive pad; and R2 is the second resistance
10 between the second conductive pad disposed on
11 the second portion and the bar-type conductive
12 pad.

1 9. The method as claimed in claim 5, wherein the
2 first to fourth conductive pads and the bar-type
3 conductive pad are made by the same material.

1 10. The method as claimed in claim 5, wherein the
2 first to fourth conductive pads and the bar-type
3 conductive pad are made of polysilicon.

1 11. The method as claimed in claim 5, wherein the
2 bar-type conductive pad, the first portion and the second
3 portion are parallel.

1 12. The method as claimed in claim 5, wherein the
2 alignment of the H-type trench capacitors and the bar-
3 type conductive pad is abnormal when the first resistance
4 does not equal the second resistance.